FIG 1

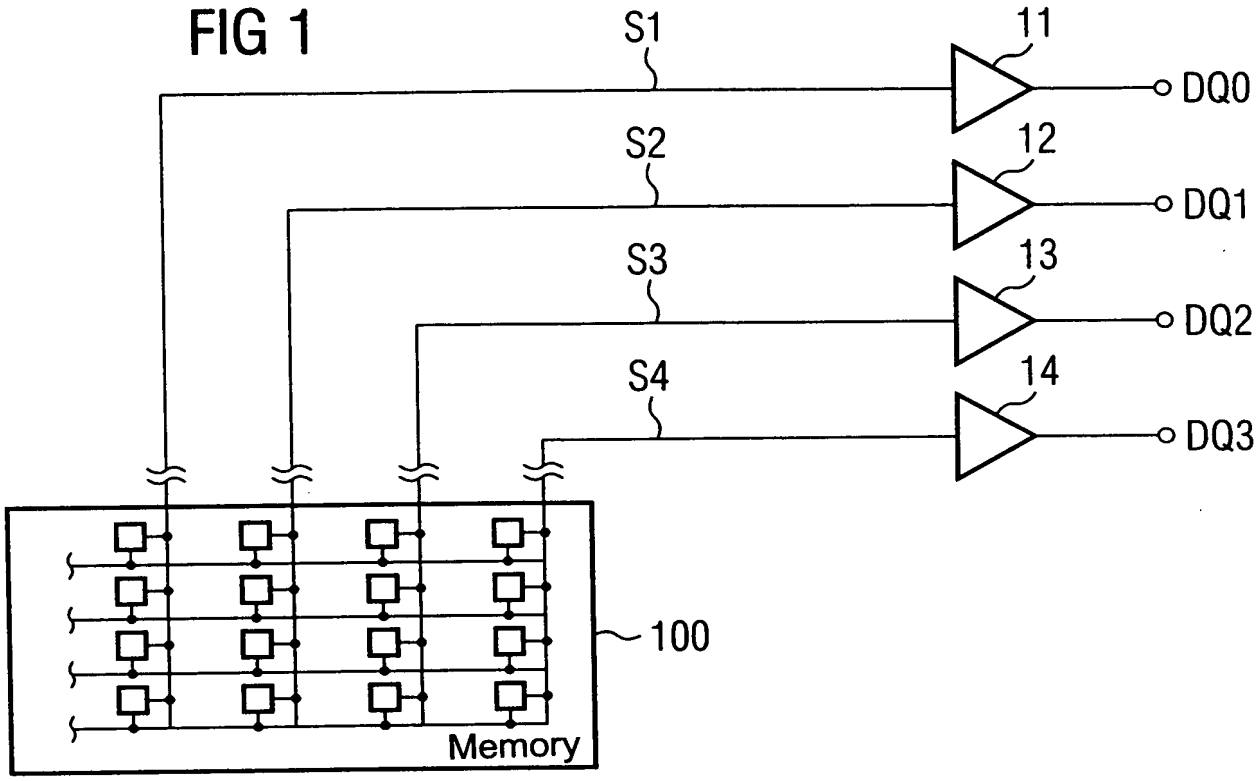
S1
11
DQ0
S2
12
DQ1
S3
13
DQ2
S4
14
DQ3
100
Memory

FIG 4

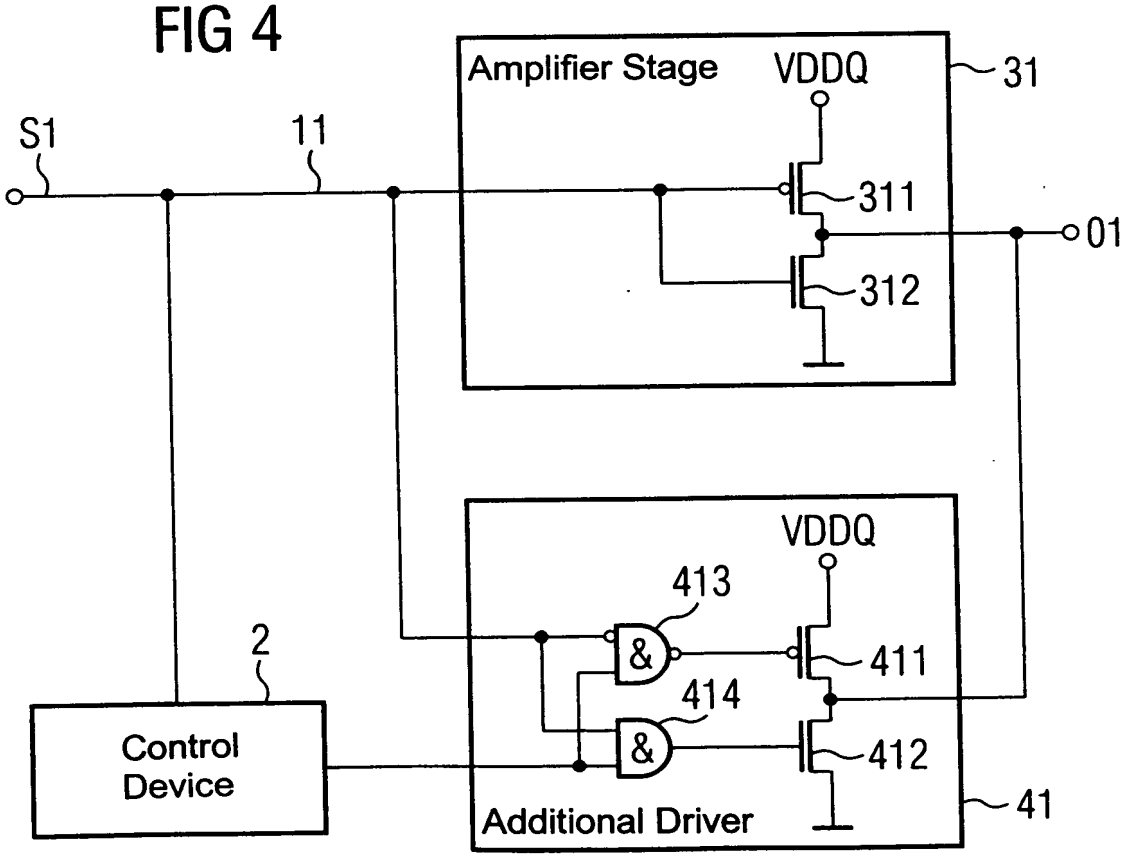
Amplifier Stage
VDDQ
31
S1
11
311
01
312
VDDQ
413
2
&
411
414
&
412
Control Device
Additional Driver
41

FIG 2

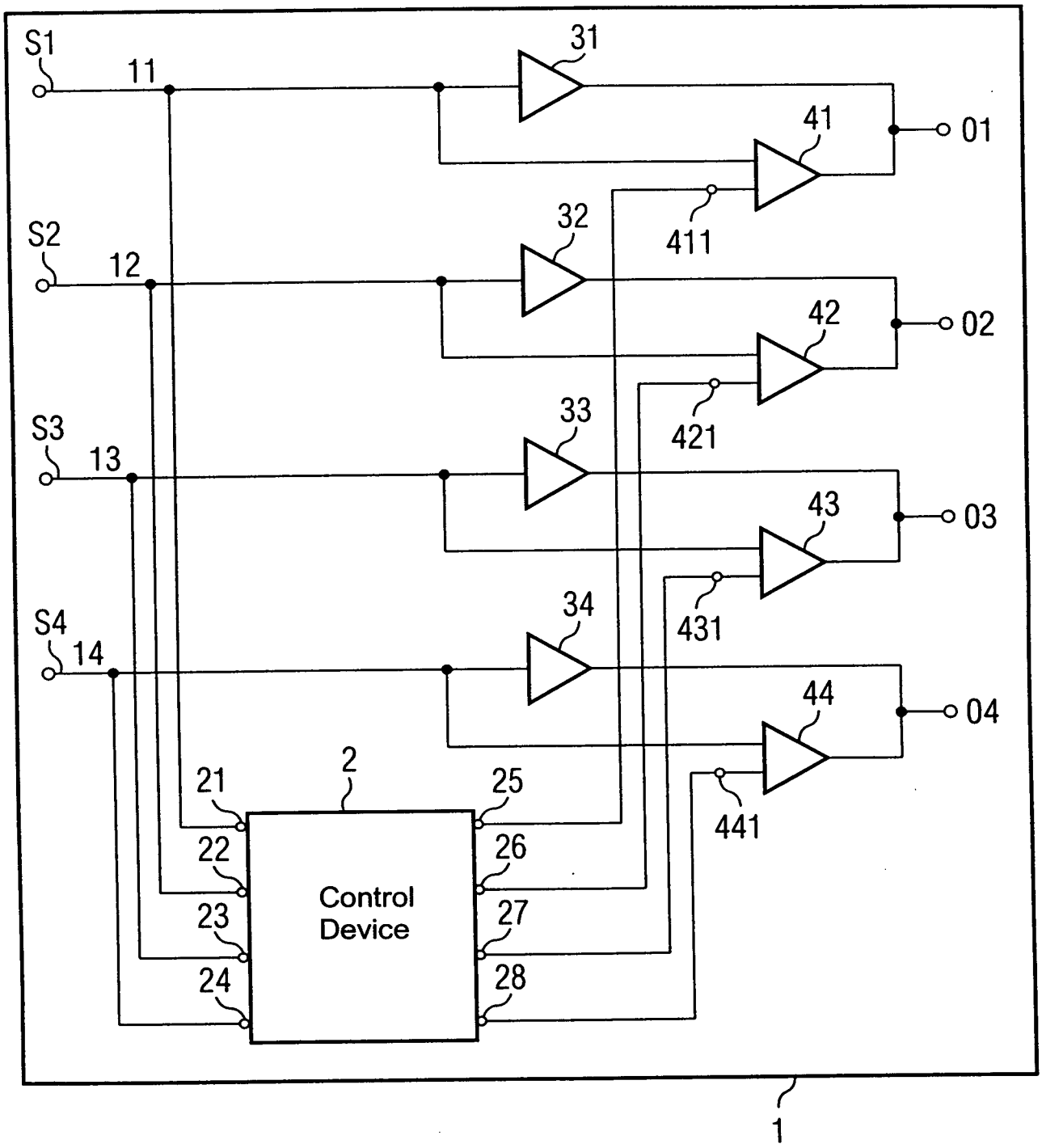
S1
11
31
41
01
411
S2
12
32
42
02
421
S3
13
33
43
03
431
S4
14
34
44
04
441
2
21
25
22
26
23
27
24
28
Control Device
1

FIG 3

SL	DW1	DW2	DW3	SZP1	SZP2	SZW1	SZW2	Control Signals Generated After Transfer DW1	Control Signals Generated After Transfer DW2	Driver Stages Transfer DW1 to DW3	Additional Driver Stages Transfer DW2	Additional Driver Stages Transfer DW3
S1	0	0	1	00	01	0	1	-	1	31=en	41=dis	41=en
S2	0	1	0	01	10	1	1	-	-	32=en	42=dis	42=dis
S3	0	0	1	00	01	0	1	-	1	33=en	43=dis	43=en
S4	0	0	0	00	00	0	0	-	-	34=en	44=dis	44=dis

301 303 305 307 309 311

302 304 306 308 310